# POWER-UP DETECTION CIRCUIT WITH LOW CURRENT DRAW FOR DUAL POWER SUPPLY CIRCUITS

## ABSTRACT OF THE DISCLOSURE

A power monitor circuit for notifying processing circuits operating from a first power supply having a VDD output voltage when a second power supply having a VDDIO output voltage is powered up, wherein VDDIO is greater than VDD. The power monitor circuit comprises: 1) a voltage divider circuit coupled between the second power supply and ground and having an output node that rises to a high voltage when the second power supply is powered up; and 2) an odd number of serially connected inverters operating from the first power supply. An input of a first of the serially connected inverters is connected to the voltage divider circuit output node and an output of a last of the serially connected inverters produces a status signal that is low when the voltage divider circuit output node is high and is high when the voltage divider circuit output node is low. The status signal is an input signal to the voltage divider circuit operable to minimize DC current consumption in the voltage divider circuit when the second power supply is powered up while maintaining a value of the status signal.